

広くASICデザインに適用中

その中におけるチップサイズ見積りの比較 (vs 実際のシリコン)

Design Description	Chip 1	Chip 2
Technology node	TSMC 90G	TSMC 65LP
Vendor, cell library	ARM	ARM
Gate count	15,015,000	7,000,000
Number of instantiated memories	423, 15.53Mbits	180, 5Mbits
IO interfaces	GPIO, SSTL, LVDS	GPIO,
List of hard IP	2 DDR2, Multiple XAUI, PCIE	Multiple XAUI, PCI-E

CCPS

CCPS estimated die size	121 sq mm	52 sq mm
Actual die size	114.45 sq mm	58.6 sq mm