

Fujitsu's CPF Based Low Power Design Status & Today's Power Format

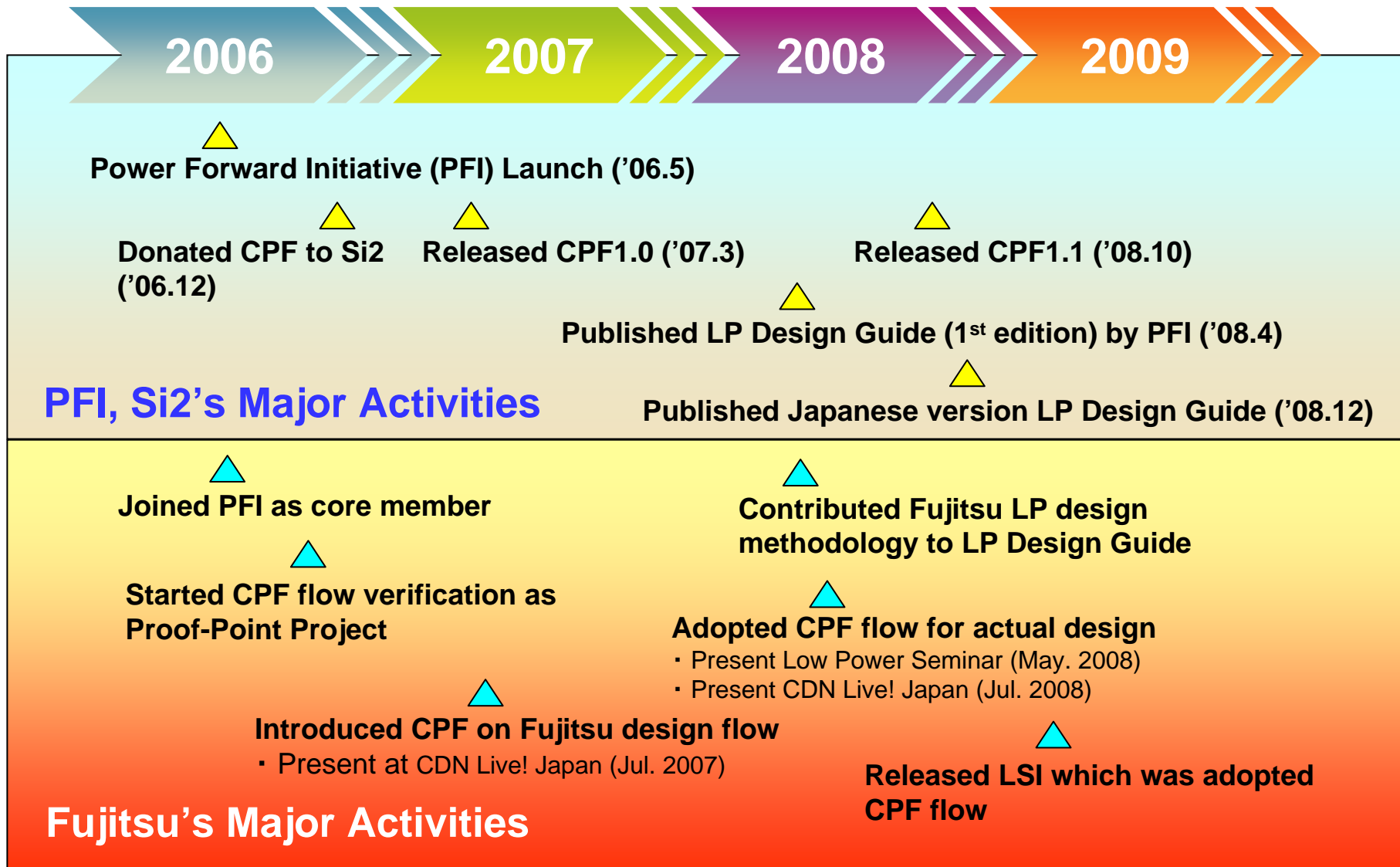
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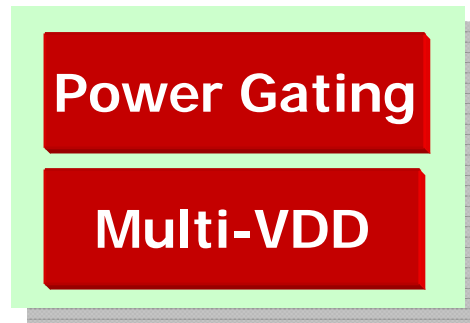
Fujitsu Microelectronics Ltd.

- Fujitsu's Low Power Design History and Results
- Fujitsu's CPF Low Power Design Flow
- CPF vs. UPF

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Low Power Design History





Conventional



- ✓ Need Expert
- ✓ Need many Work-Around

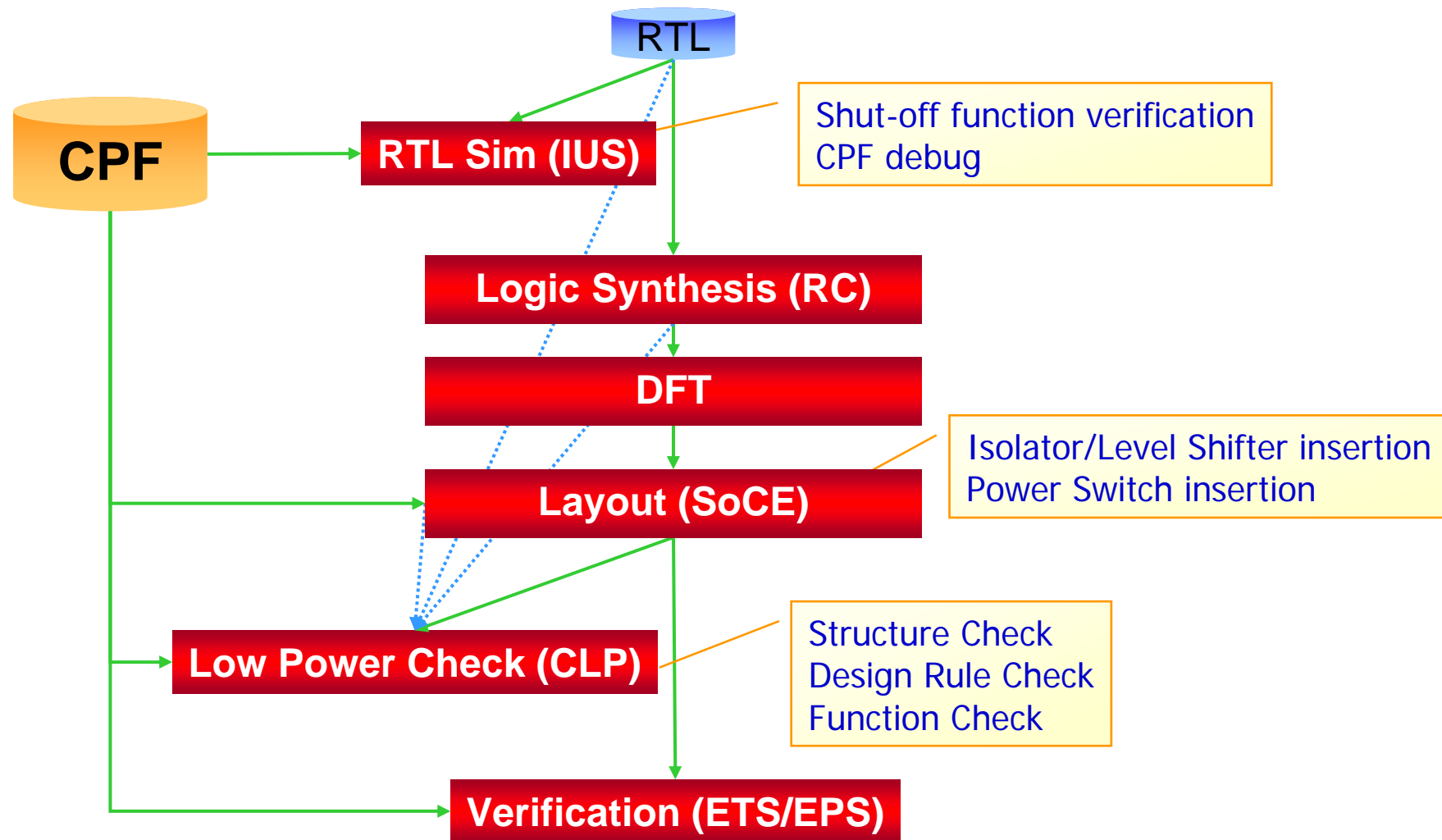
CPF Adoption



Enable short TAT due to easy to design

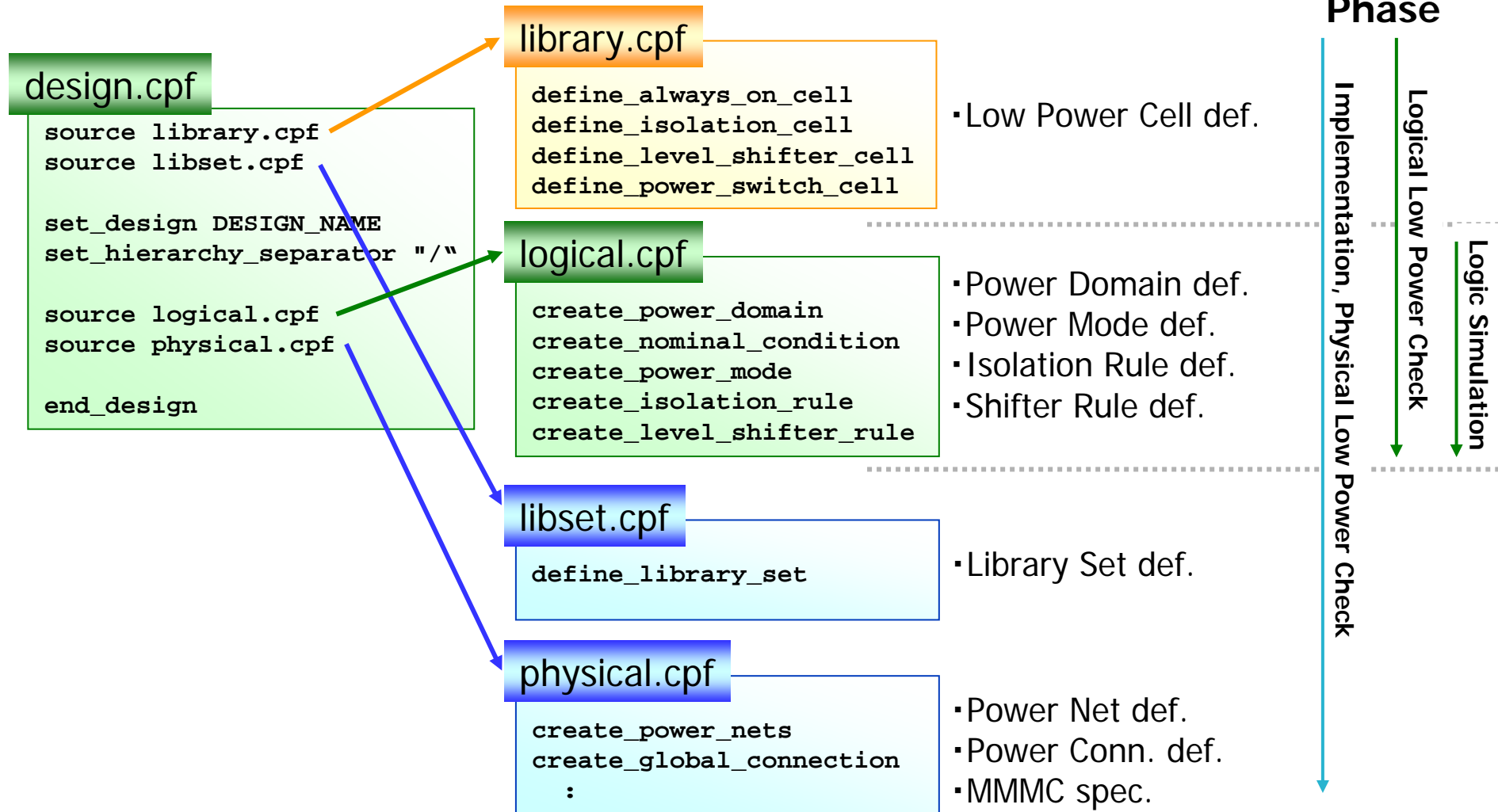
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CPF Low Power Design Flow



CPF (Common Power Format)

- Describes Power Intent as LSI Specification.
- Describes Power Intent depending on a design phase.



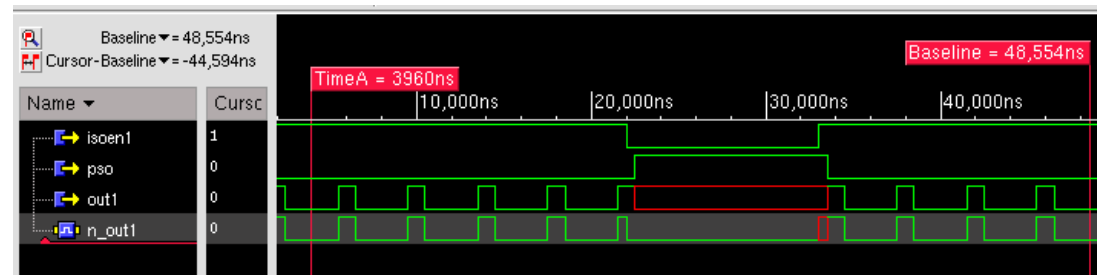
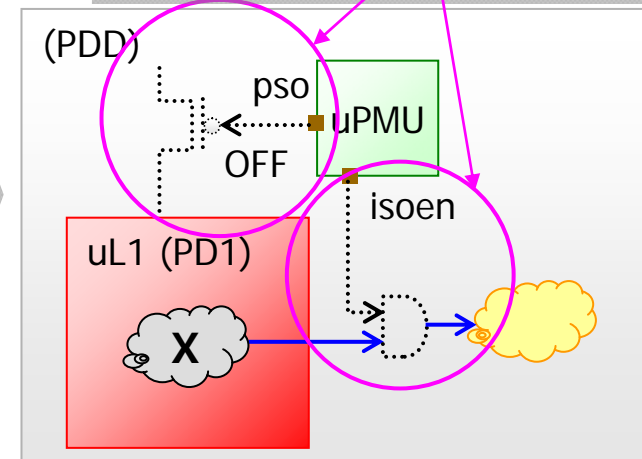
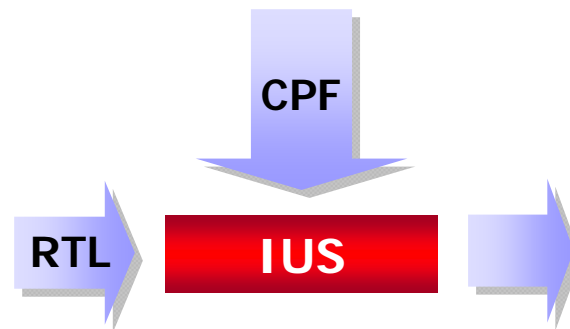
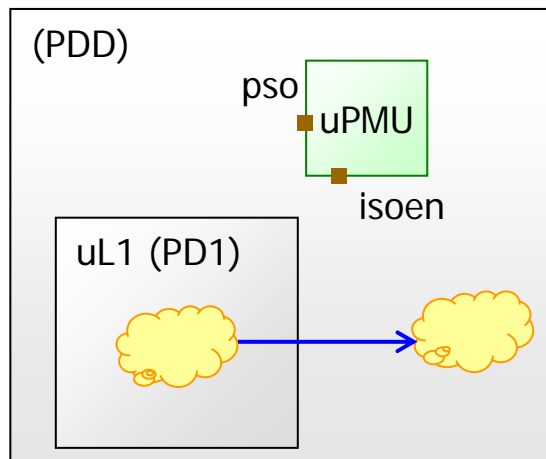
Shut-off Simulation with CPF

- Just prepare logical.cpf to run shut-off simulation.

```

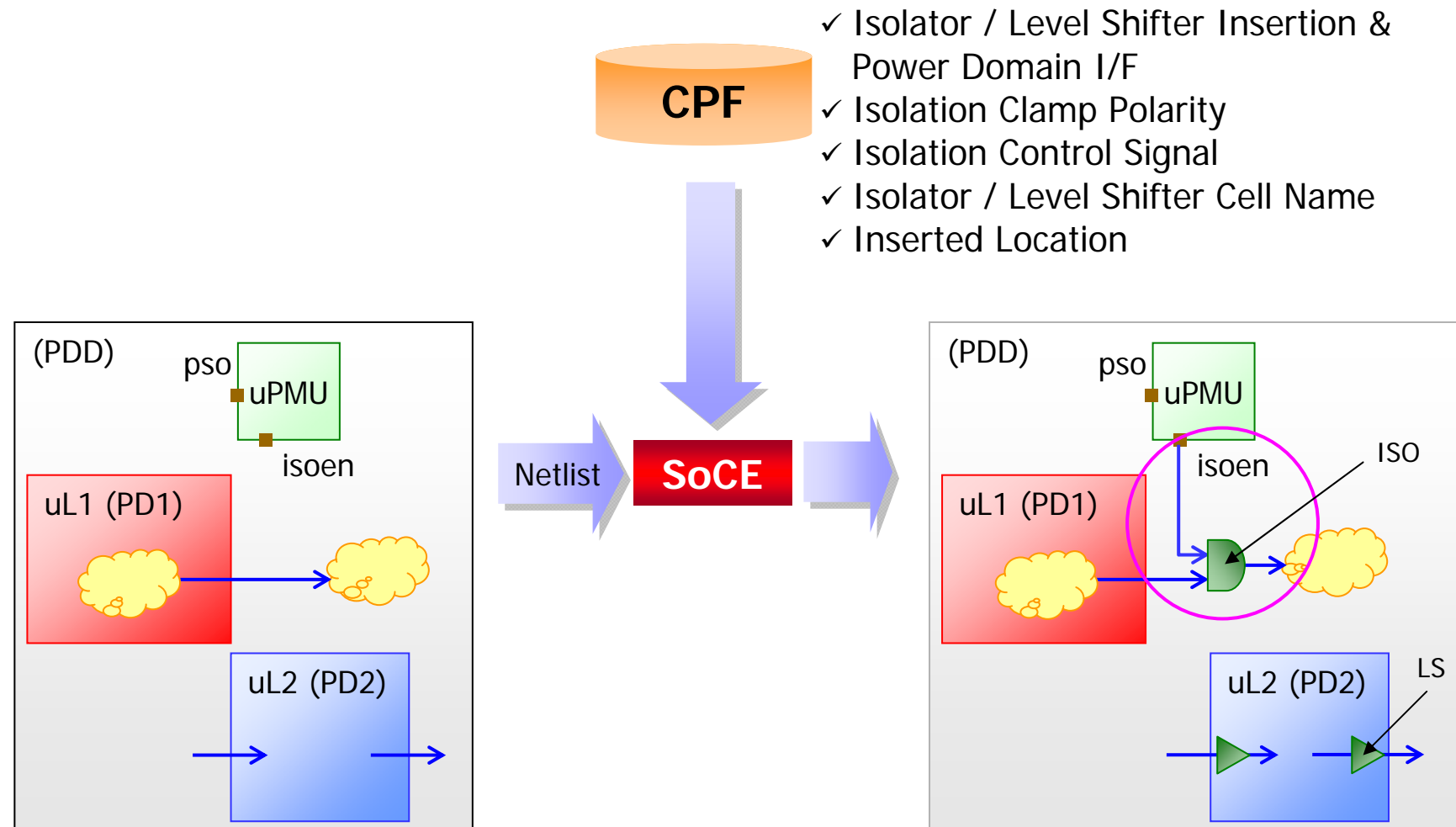
create_power_domain -name PDD -default
create_power_domain -name PD1 -instances uL1 -shutoff_condition uPMU/ps0
create_isolation_rule -name ISO_PD1 -from PD1 ¥
                    -isolation_output low -isolation_condition !uPMU/isoen
create_nominal_condition -name ON12 -voltage 1.2
create_power_mode -name PM1 -domain_conditions {PDD@ON12 PD1@ON12} -default
create_power_mode -name PM2 -domain_conditions {PDD@ON12}
    
```

Verify X prop. & clamp signal with virtual PSW & Isolator



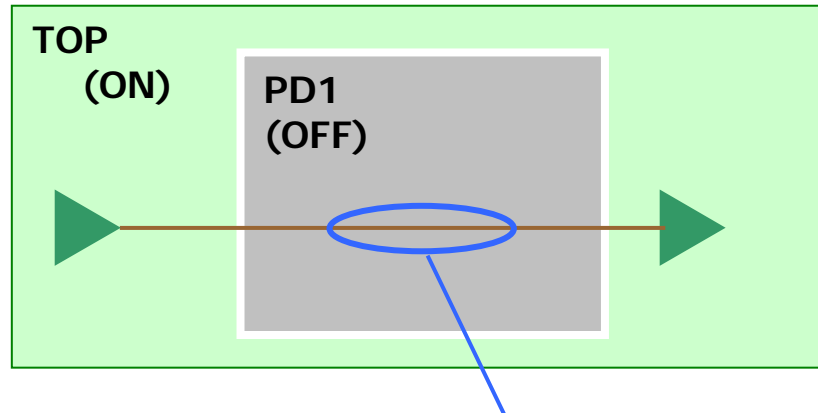
Isolator / Level Shifter Insertion

- Isolator / Level Shifter are automatically inserted according to CPF spec. by loading netlist and CPF to SoCE.



Logic and Physical Interface

- All design intents are not always described in CPF.

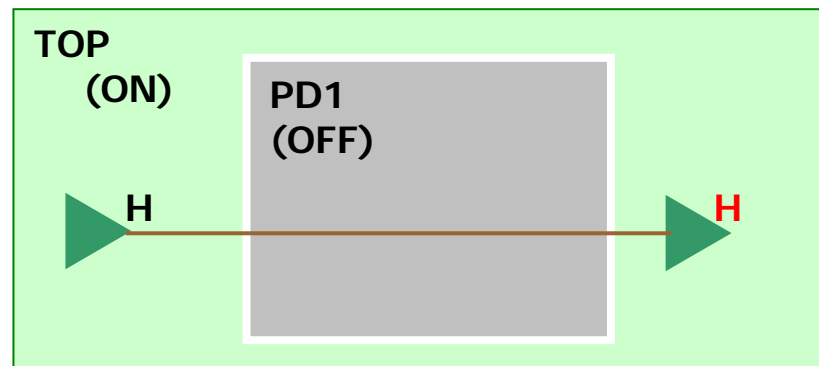


Depending on the option of the simulator, it can handle this signal as a buffer or as a net.

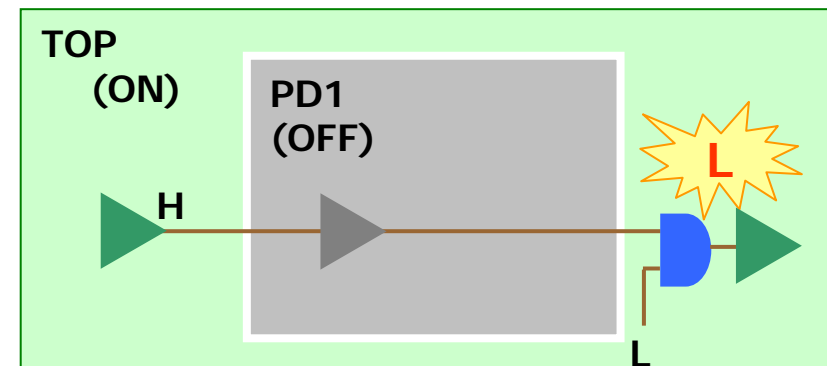


There is a risk that CPF can not transfer design intent to implementation properly.

As a net

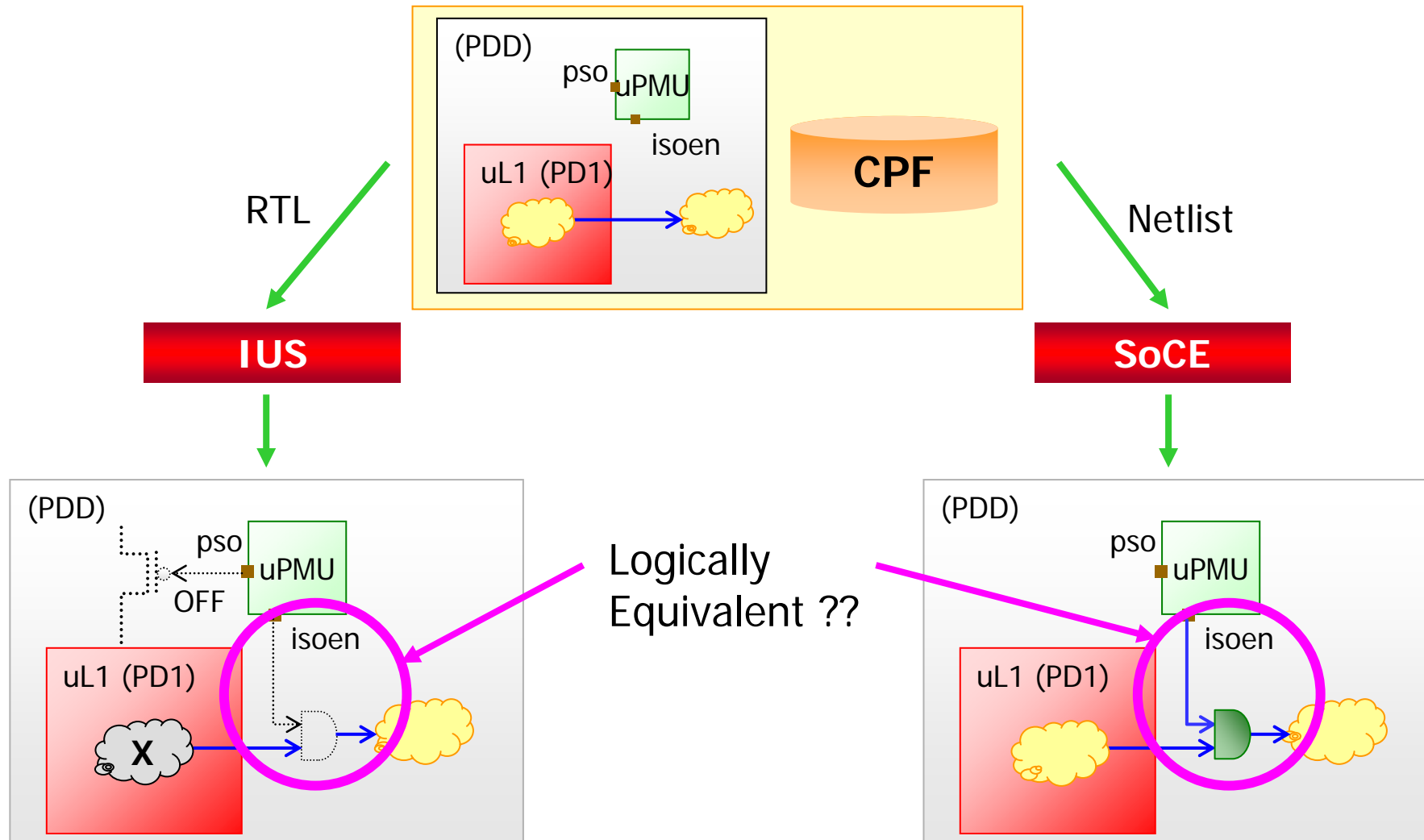


As a buffer



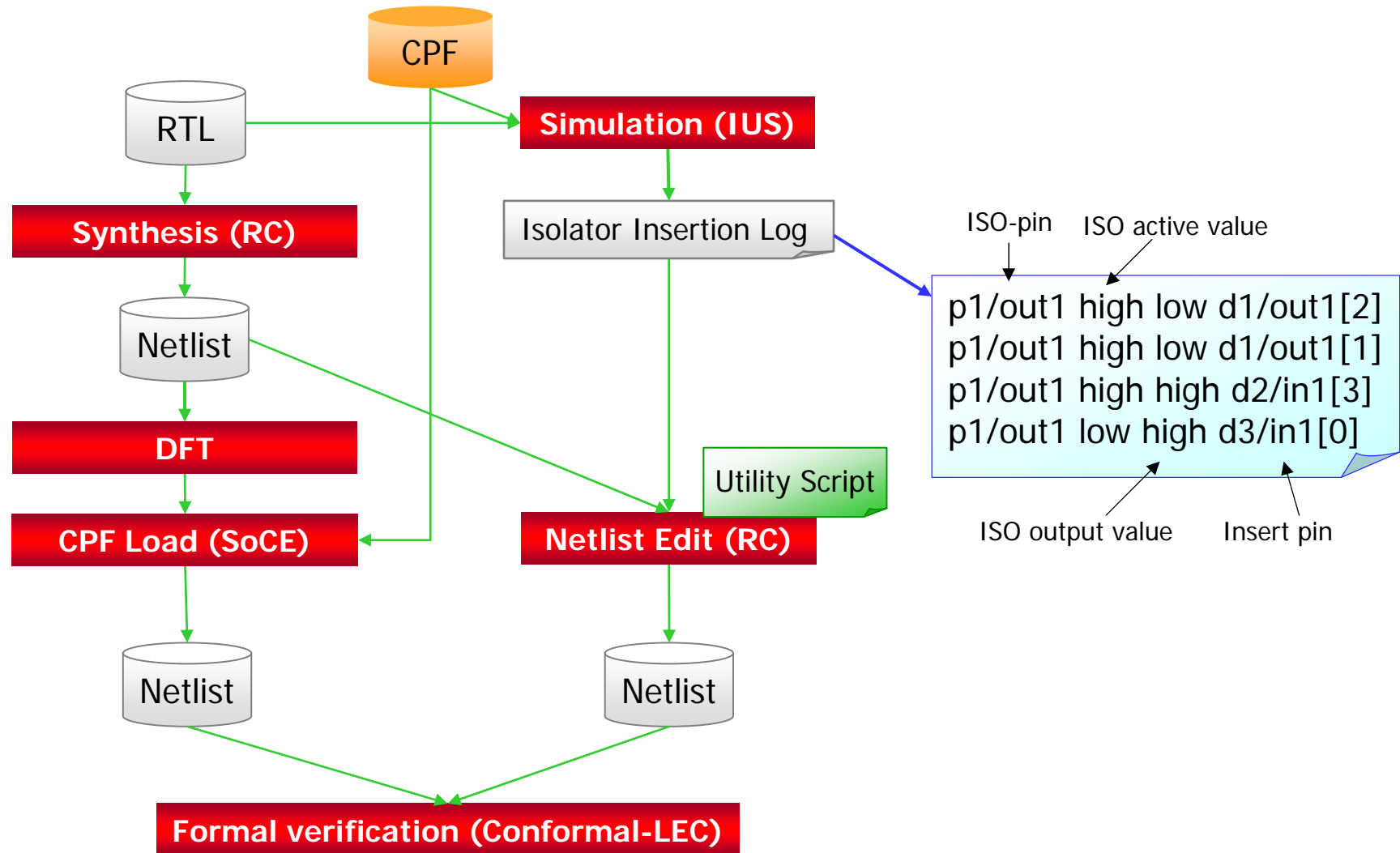
Isolation logic equivalence check (1)

- Need to verify equivalence between Isolators inserted by SOCE and Isolators virtually inserted by RTL simulation.



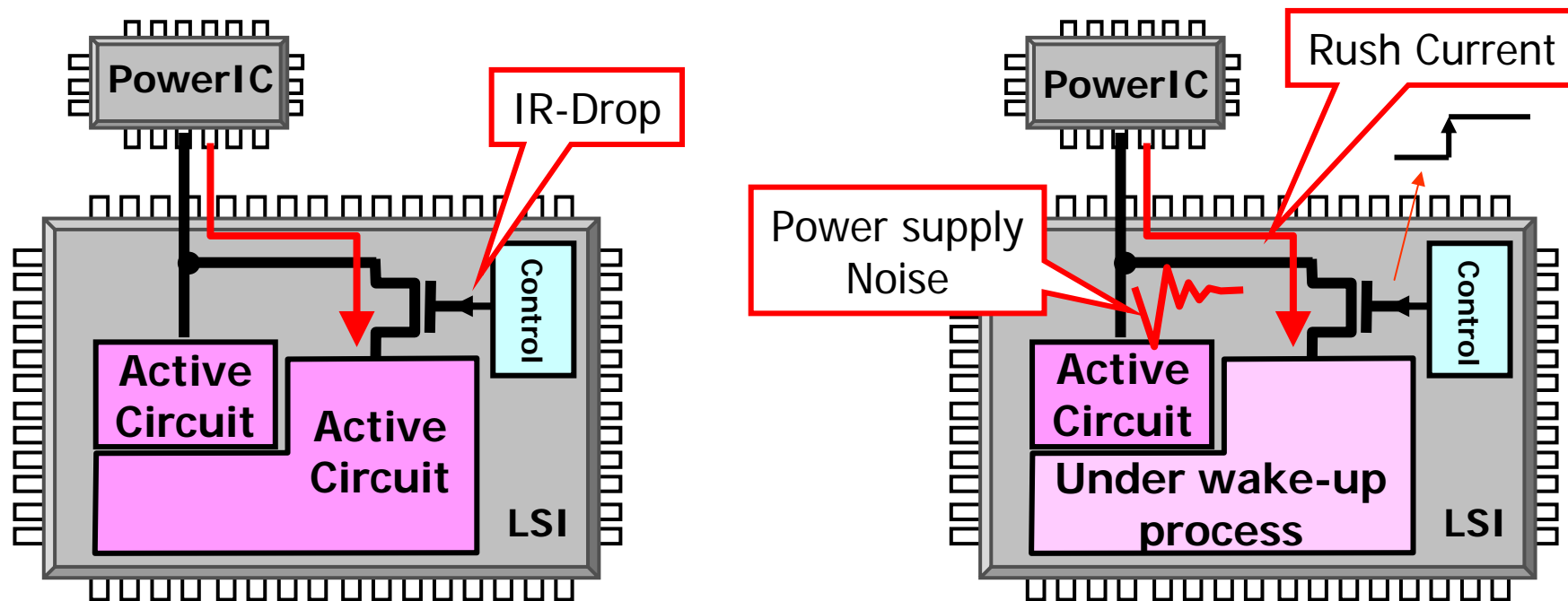
Isolation logic equivalence check (2)

Virtual Isolator (in RTL simulation) verification flow



■ The challenges of On Chip Power Gating

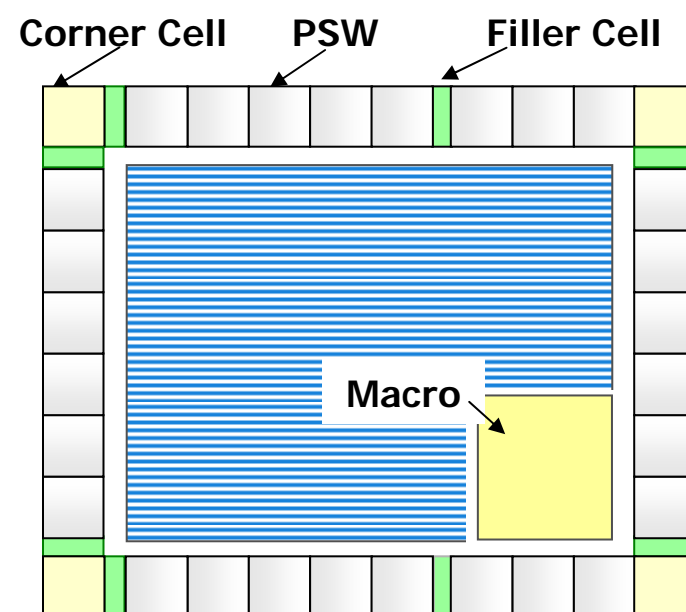
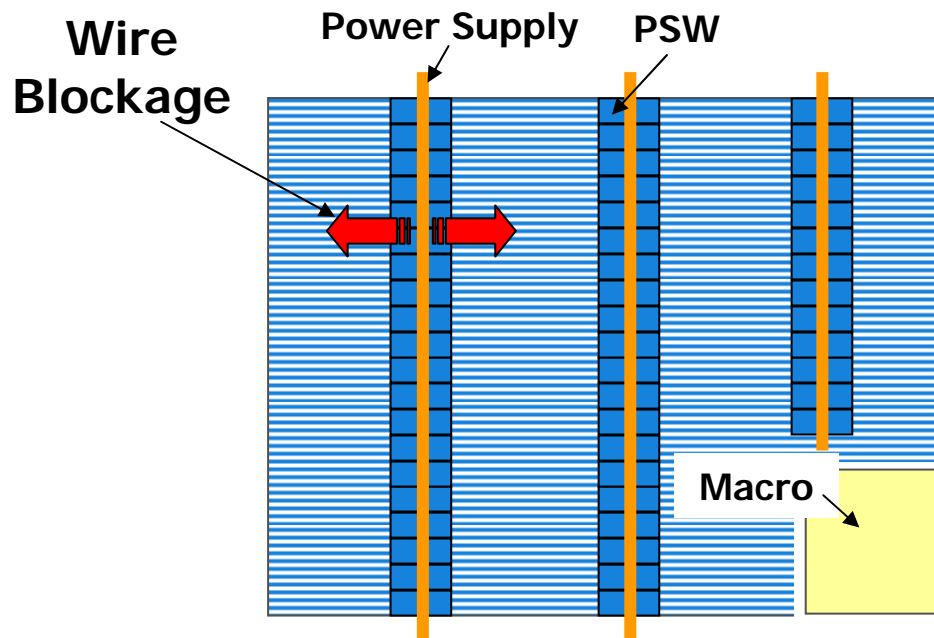
- Supplying enough current to the circuit, realizing small IR-Drop.
- Controlling Rush current when Power Switches are turned on.



Control of appropriate Power Switch and adjustment of the size are important

COLUMN Type Power Switch vs. RING Type Power Switch

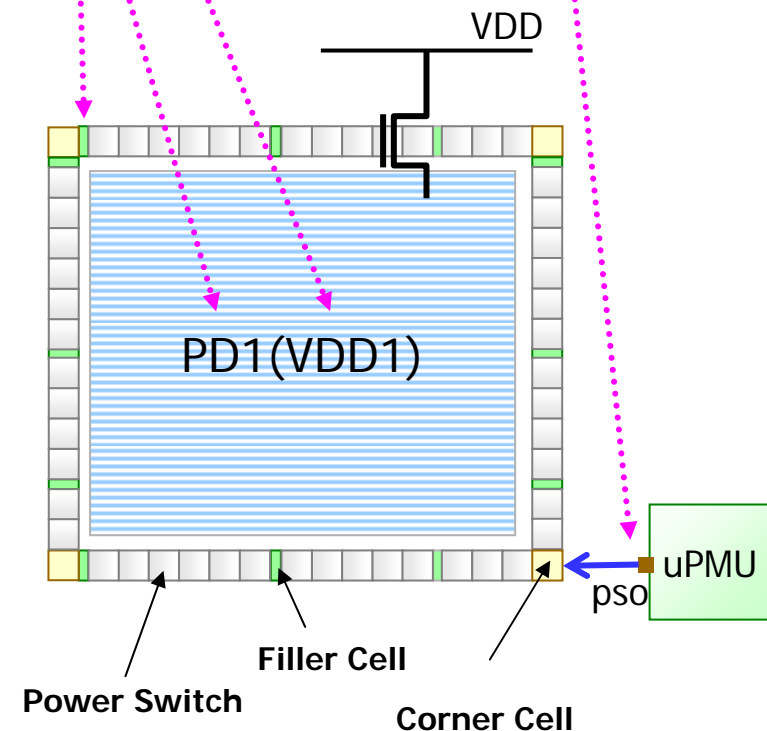
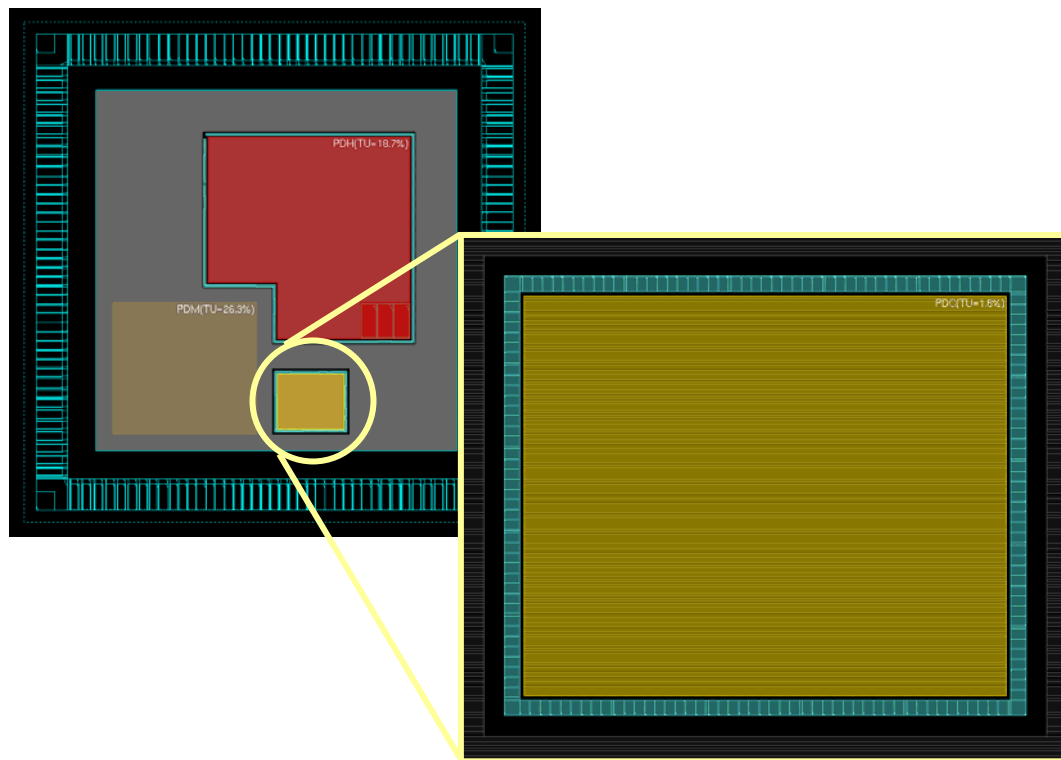
	COLUMN Type PSW	RING Type PSW
Area efficiency	■ Tr size is small	◆ Tr size is large
Routing efficiency	■ PSW prevents horizontal routing	◆ No routing restriction inside Power Domain
Hard IP	■ Not applicable ■ Need to re-create physical design for power shut-off	◆ Easy to re-use for power shut-off



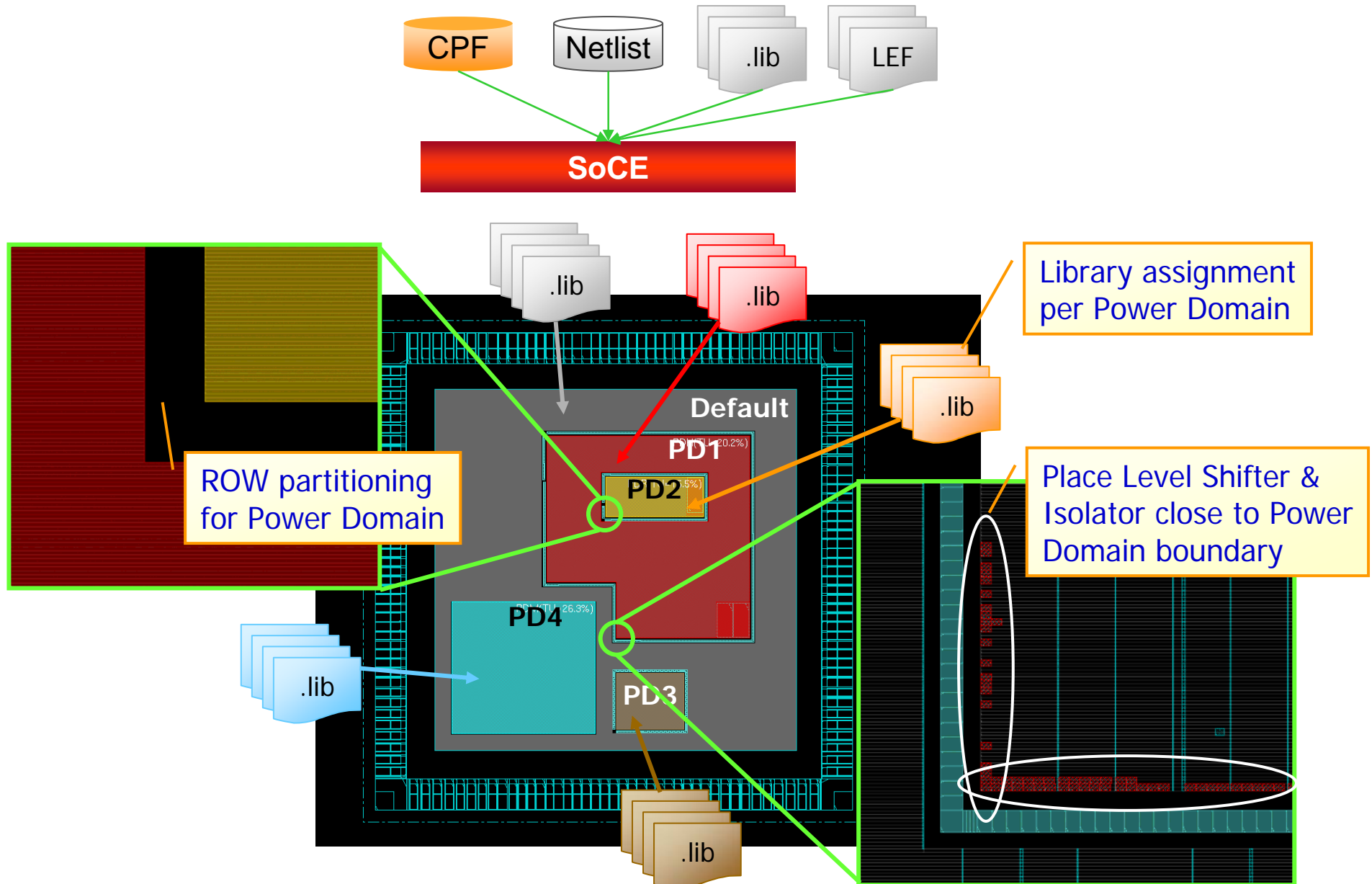
Power Switch Insertion and Placement

- SOCE can insert & place PSW automatically & accurately based on the specification in CPF

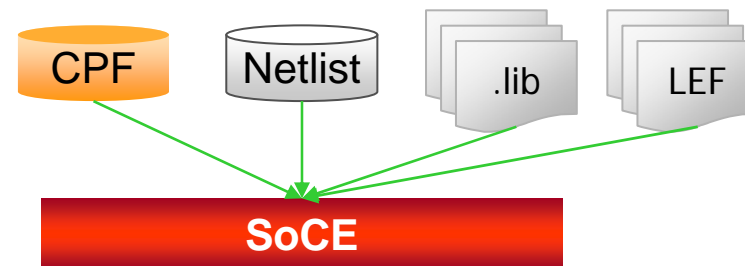
```
update_power_domain -name PD1 -primary_power_net VDD1
create_power_switch_rule -name PSW_PD1 -domain PD1 -external_power_net VDD
update_power_switch_rule -name PSW_PD1 -cells PSWCELL ¥
                        -prefix PSW_PD1_ -enable_condition_1 {!uPMU/ps0}
```



Power Domain Aware P&R (1)

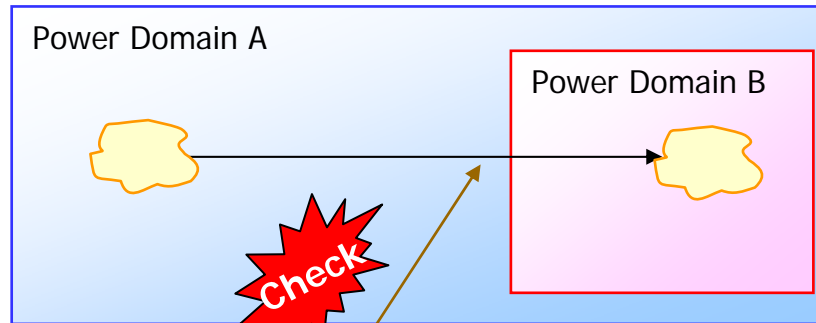


Power Domain Aware P&R (2)

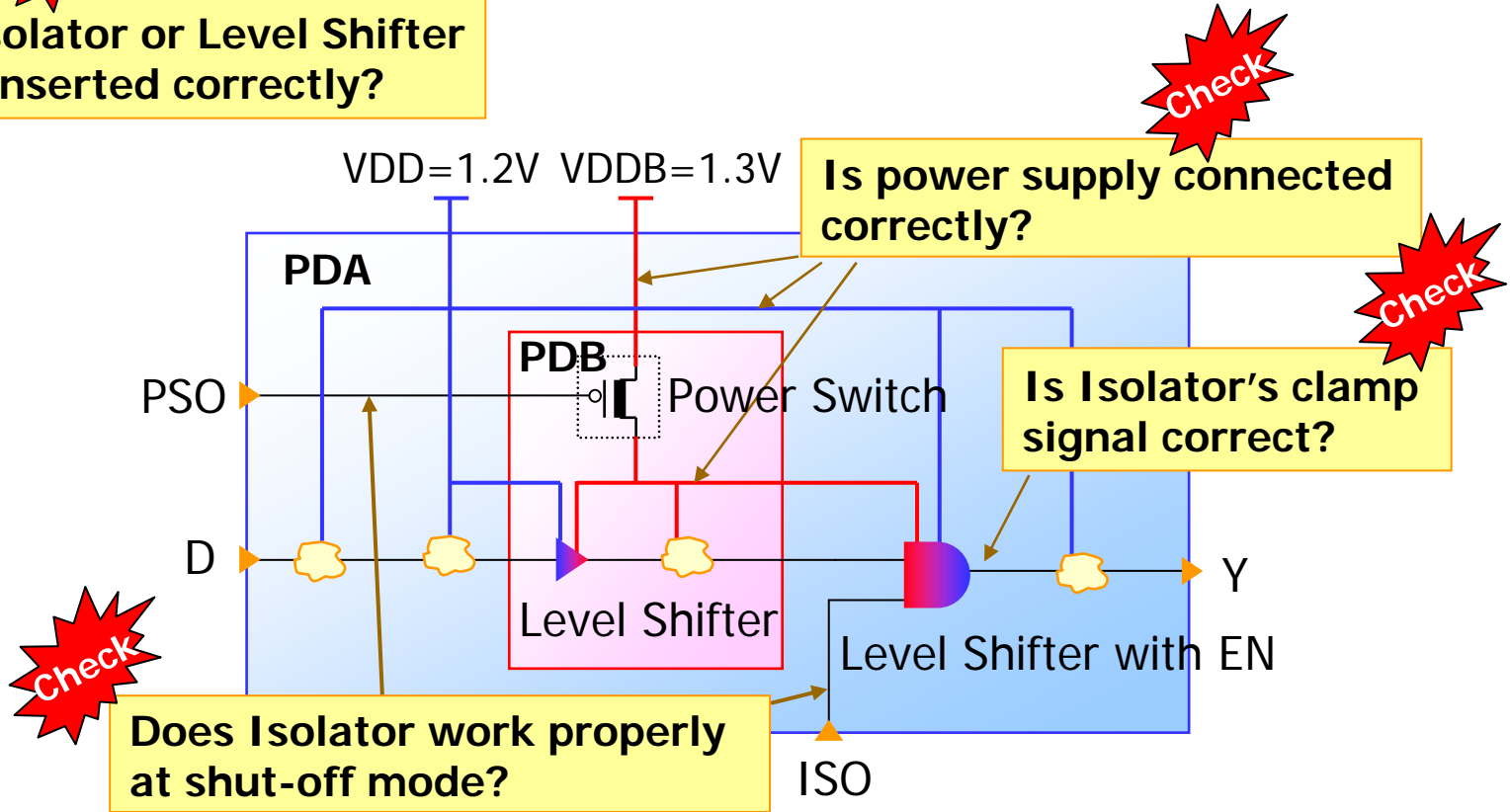


- Placement (Std Cell Placement, Scan-Reorder)
- Optimization (according to Power Domain and ISO/LS Rule)
- Multi-Mode/Multi-Corner Optimization (can be defined in CPF)
- CTS (keep Power Domain Ports)
- Routing (w/i Power Domain, Antenna Diode insertion, tie-high/low conn.)
- Physical Cell Placement (Decap, Well Tap, Filler)

Low Power Check (1)

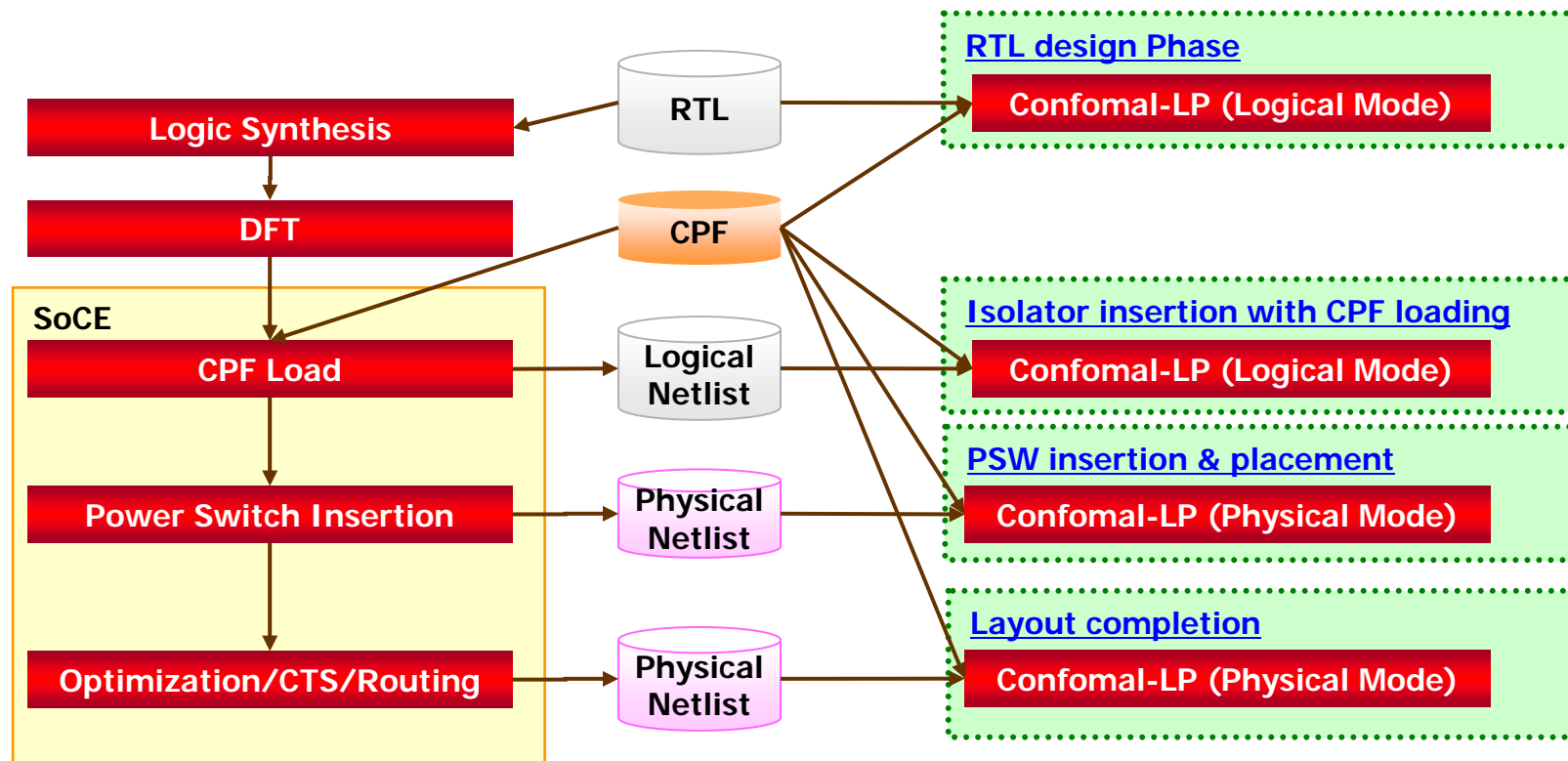


Is Isolator or Level Shifter inserted correctly?



Low Power Check (2)

- Conformal-LP verifies Low Power structure and function
 - Is Isolator or Level Shifter inserted correctly?
 - Is Isolator's Clamp signal correct?
 - Is power supply connected correctly?
 - Does Isolator work properly at shut-off mode?



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Specification

CPF

- Both syntax and semantics are managed by Si2.
- Spec. is relatively released earlier, since it is determined by Si2 LPC members only.
- Easy to understand due to simple specification.
- Easy to deploy in a Multi Vendor Flow.

UPF

- Syntax is managed by Accellera & IEEE, but semantics are not managed.
- Comprehension of commands and support area are different per vendors.
- Spec. release is slow, since it is determined by many IEEE members.
- Difficult to understand due to ambiguous specification.
- Difficult to deploy in a Multi Vendor Flow.

Usability

CPF

- Logic part and physical part can be separated clearly per design phase.
- RTL Simulation can be run with only logic part.
- Easy to deploy for ASIC business.
- Easy to write and understand due to consistent command naming rule such as "create_*" for the rule definition, "update_*" to specify physical info and "set_*" for variable definition.

UPF

- Need to describe physical information such as Power net name, Power Port name, Power Switch connection at RTL design phase.
- Difficult to deploy for ASIC business.
- Difficult to write and understand the usage and semantics from the command name.

Comparison description for RTL design

CPF

```
create_power_domain -name PD0 -default
create_power_domain -name PD1 -instances uL1 ¥
    -shutoff_condition uPMU/ps0
create_isolation_rule -name ISO_PD1 -from PD1 ¥
    -isolation_condition uPMU/isoen
create_nominal_condition -name ON -voltage 1.2
create_power_mode -name PM1 -domain_conditions {
    PD0@ON PD1@ON } -default
create_power_mode -name PM2 -domain_conditions {
    PD0@ON }
```

Simple &
less code size

UPF

```
create_power_domain PD0
create_power_domain PD1 -elements uL1
create_supply_port VDD -direction in
create_supply_net VDD -domain PD0
create_supply_net VDD -domain PD1 -reuse
connect_supply_net VDD -ports VDD
create_supply_port VSS -direction in
create_supply_net VSS -domain PD0
create_supply_net VSS -domain PD1 -reuse
connect_supply_net VSS -ports VSS
create_supply_port VDD1 -direction out
create_supply_net VDD1 -domain PD0
create_supply_net VDD1 -domain PD1 -reuse
connect_supply_net VDD1 -ports VDD1
set_domain_supply_net PD0 -primary_power_net VDD ¥
    -primary_ground_net VSS
set_domain_supply_net PD1 -primary_power_net VDD1 ¥
    -primary_ground_net VSS
create_power_switch PSW_PD1 ¥
    -domain PD1 ¥
    -input_supply_port {VDIN VDD} ¥
    -output_supply_port {VDOUT VDD1} ¥
    -control_port {IN uPMU/ps0} ¥
    -on_state {state VDIN {IN}}
set_isolation ISO_PD1 ¥
    -domain PD1 ¥
    -isolation_power_net VDD ¥
    -clamp_value 0 ¥
    -applies_to outputs
set_isolation_control ISO_PD1 ¥
    -domain PD1 ¥
    -isolation_signal uPMU/isoen ¥
    -isolation_sense low ¥
    -location parent
add_port_state VDD -state {ON 1.2}
add_port_state VDD1 -state {ON 1.2} -state {OFF off}
create_pst PST -supplies {VDD VDD1}
add_pst_state PM1 -pst PST -state {ON ON}
add_pst_state PM2 -pst PST -state {ON OFF}
```

Too many
codes

Tool Support

CPF

- Practical for actual design project. (already in the brush-up phase)
- Accurate behavior according to power intent specification in CPF.
- Supports Ring Type Power Switch.

UPF

- In many case, Tool's native commands are used instead of UPF information to implement Low Power technique.
- Some tools can not distinguish between its native commands and UPF commands.
- No support of Ring Type Power Switch.

Flow

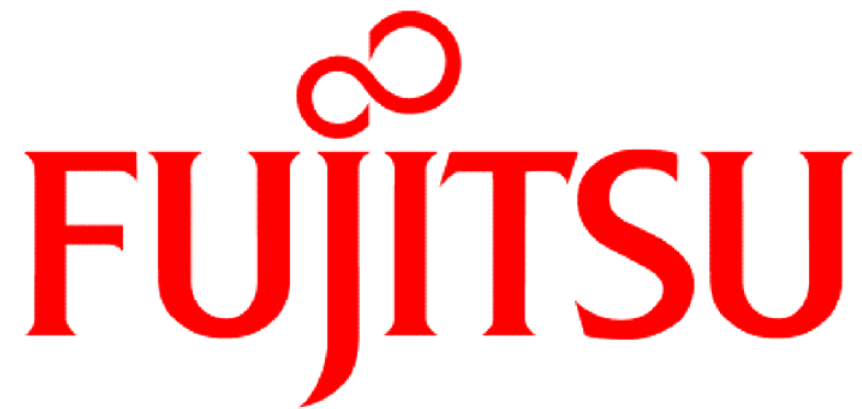
CPF

- Can keep using CPF, which was verified at the logic design phase, as a golden CPF throughout the design flow.

UPF

- Need UPF equivalence checking at each design phase, since UPF is modified at each design phase.

- Fujitsu developed a reliable Low Power design flow by adopting CPF ahead of the world-wide.
 - Fujitsu appreciates Cadence's effort and expects further cooperation.
- CPF is more practical and has the quality to be de facto standard as Power Format comparing UPF. Fujitsu is expecting further progress of CPF.



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THE POSSIBILITIES ARE INFINITE